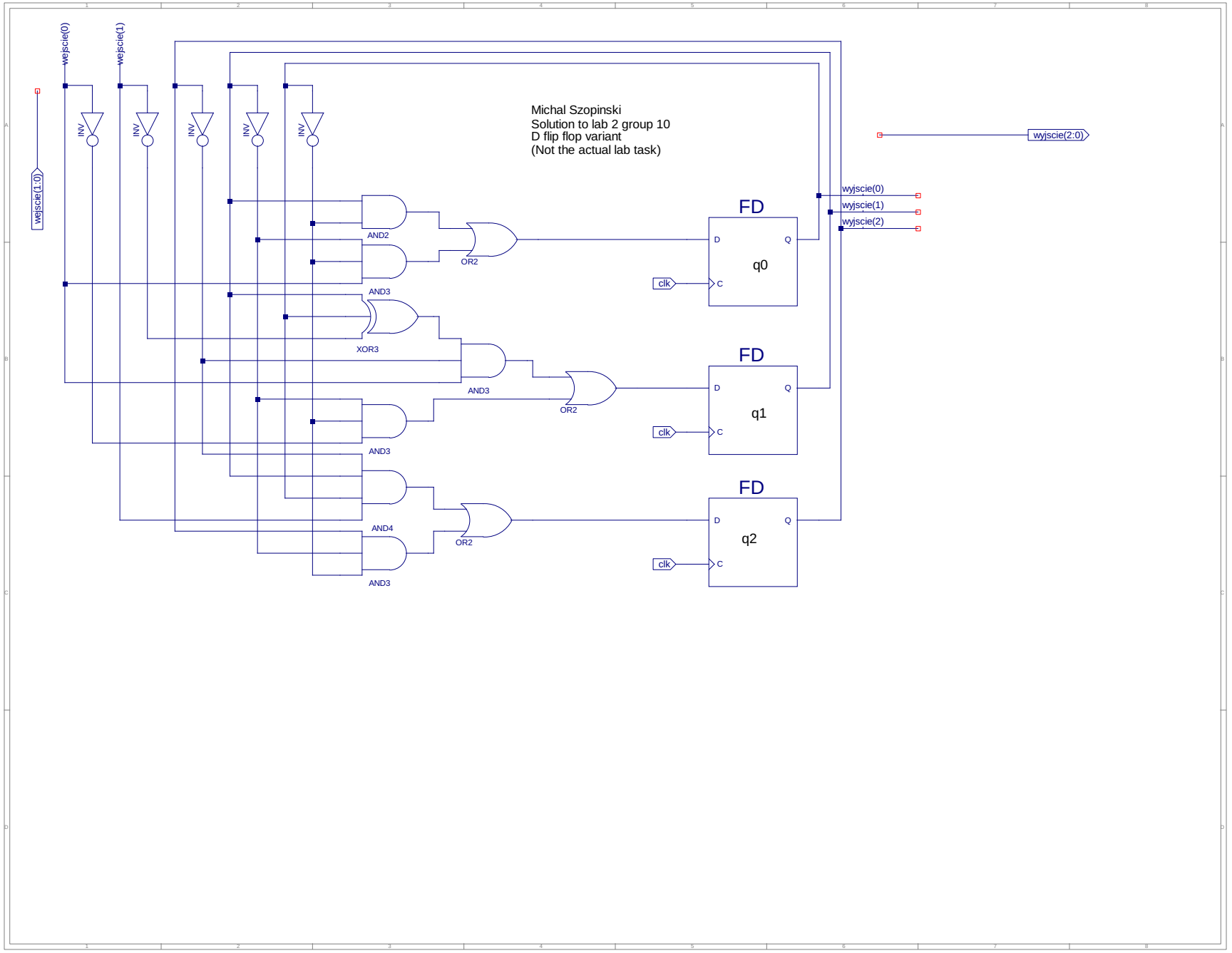
wejscie(0)
wejscie(1)
wejscie(1:0)
INV
INV
INV
INV
INV
Michal Szopinski
Solution to lab 2 group 10
D flip flop variant
(Not the actual lab task)
wyjscie(2:0)
wyjscie(0)
wyjscie(1)
wyjscie(2)
AND2
OR2
AND3
XOR3
AND3
OR2
AND3
AND4
OR2
AND3
FD
D
Q
q0
C
clk
FD
D
Q
q1
C
clk
FD
D
Q
q2
C
clk

```
1   -- Vhdl test bench created from schematic
    /home/mszopinski/Desktop/labko2d/schem.sch - Tue Dec  3 23:15:26
    2019
2   --
3   -- Notes:
4   -- 1) This testbench template has been automatically generated
    using types
5   -- std_logic and std_logic_vector for the ports of the unit under
    test.
6   -- Xilinx recommends that these types always be used for the
    top-level
7   -- I/O of a design in order to guarantee that the testbench will
    bind
8   -- correctly to the timing (post-route) simulation model.
9   -- 2) To use this template as your testbench, change the filename
    to any
10  -- name of your choice with the extension .vhd, and use the
    "Source->Add"
11  -- menu in Project Navigator to import the testbench. Then
12  -- edit the user defined section below, adding code to generate the
13  -- stimulus for your design.
14  --
15  LIBRARY ieee;
16  USE ieee.std_logic_1164.ALL;
17  USE ieee.numeric_std.ALL;
18  LIBRARY UNISIM;
19  USE UNISIM.Vcomponents.ALL;
20  ENTITY schem_schem_sch_tb IS
21  END schem_schem_sch_tb;
22  ARCHITECTURE behavioral OF schem_schem_sch_tb IS
23
24     COMPONENT schem
25     PORT( clk    :  IN STD_LOGIC;
26           wyjscie :  OUT   STD_LOGIC_VECTOR (2 DOWNTO 0);
27           wejscie :  IN STD_LOGIC_VECTOR (1 DOWNTO 0));
28     END COMPONENT;
29
30     SIGNAL clk  :  STD_LOGIC;
31     SIGNAL wyjscie :  STD_LOGIC_VECTOR (2 DOWNTO 0);
32     SIGNAL wejscie :  STD_LOGIC_VECTOR (1 DOWNTO 0);
33
34  BEGIN
35
36     UUT: schem PORT MAP(
37        clk => clk,
```

```
38          wyjscie => wyjscie,
39          wejscie => wejscie
40       );
41
42    -- *** Test Bench - User Defined Section ***
43       tb : PROCESS
44
45       procedure flashClock is
46       begin
47          for i in 1 to 30 loop
48             clk <= not clk;
49             wait for 1 ns;
50          end loop;
51       end procedure;
52
53       BEGIN
54          -- set input
55          clk <= '1';
56          wejscie <= "00";
57          wait for 10 ns;
58
59          -- mod 3 down
60          wejscie <= "01";
61          flashClock;
62          wait for 10 ns;
63
64          -- mod 4 down
65          wejscie <= "10";
66          flashClock;
67          wait for 10 ns;
68
69          -- mod 6 up
70          wejscie <= "11";
71          flashClock;
72          wait for 10 ns;
73
74          WAIT; -- will wait forever
75       END PROCESS;
76    -- *** End Test Bench - User Defined Section ***
77
78    END;
79
```